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Review on Multilevel Inverter Topologies

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Abstract: *The only constant in industry is the change in technology. One of the major inventions which invoked this change is inverters. Power electronic devices which convert DC power into AC power at desired output voltage and frequency is known as an inverter. The output voltage of a power inverter is to be a pure sinusoidal waveform with minimum distortion, which is practically difficult to obtain. In order to make pure sinusoidal waveform from the inverter with minimum distortion the concept of multilevel inverters was introduced. A stepped voltage waveform is generated with the use of number of DC voltage sources as the input and by appropriate arrangement of the power semiconductor-based devices. Several topologies of multilevel inverters are discussed here. These find their application in traction, HVDC transmission, etc.*

I. Introduction

In recent years, the world is getting industrialized. Several industrial applications require sinusoidal waveforms with minimum distortion at a high power. For medium and high power applications, it is difficult to depend on a single switch. Therefore,the concept of multilevel inverters where introduced in 1974[2]. The basic concept of a multilevel converter is to achieve higher power using power semiconductor switches in combination with several low voltage DC sources and to perform the required power conversion by synthesizing a staircase voltage waveform. It provides flexibility in interfacing capacitors, batteries, or even renewable energy sources such as wind energy, photovoltaic energy and fuel cells as the DC voltage sources. The various combinations of these power switches aggregate the sources. The integral multiple of this forms stepped like voltage waveform of high power at the output side. Subsequently on the basis of this concept, several multilevel converter topologies have been developed[3]-[10].

A multilevel converter has several advantages over the conventional two-level converter that uses high switching frequency pulse width modulation(PWM). These features can be summarised as below [11]:

- **Staircase waveform quality:**Multilevel converter not only can generate the output voltage with very low distortion but also can reduce the dv/dt stresses; therefore the electromagnetic compatibility(EMC) problems can be reduced.
- **Common – Mode (CM) Voltage:** Multilevel converter produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies such as that proposed in [12]
- **Input Current:** Multilevel converters can draw input current with low distortion
- **Switching frequency:** Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM.

The multilevel converters are divided into two based on the number of DC supply sources used as:

- Common DC Source
- Separate DC Source

Of these the common DC source is further divided into:

- Diode Clamped Multilevel Inverter (DC-MLI)
- Flying Capacitor Multilevel Inverter (FC-MLI)

The Separate DC Source Multilevel Inverter is commonly known as Cascaded H-Bridge Multilevel Inverter (CHB-MLI). It can be of two types with equal DC sources and with unequal DC sources. This has been showcased in fig 1. The several topologies of the MLI have been studied here.

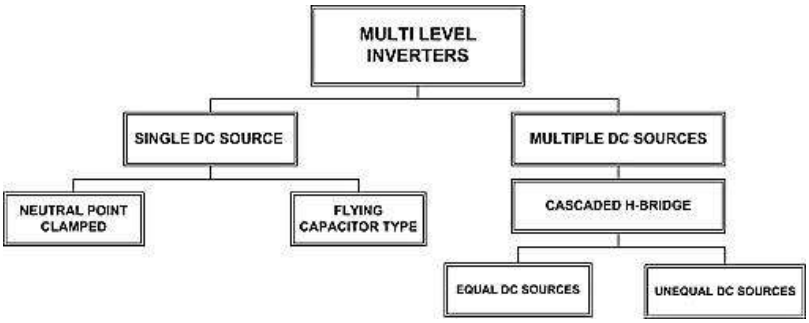

Fig 1: Taxonomy of Multilevel Inverters

II. Diode Clamped Multilevel Inverter

The diode-clamped multilevel inverter(DC – MLI) is also known as the neutral-pointclamped inverter (NPC)and was introduced by Nabae et al in the year 1981.It consists of two pairs of series switches (upper and lower) in parallel with two series capacitors where the anode of the upper diode and cathode of the lower diode is connected to the midpoint of the capacitors. This divides the main DC voltage into smaller voltages, which is shown in fig 2. The middle point of the two capacitors can be named as the "neutral point". The DC – MLI uses a single dc bus that is subdivided into a number of voltage levels by a series connection of capacitors. For a three-level diode-clamped inverter if the point C is taken as the ground reference, the output voltage has three states 0, $1/2V_{dc}$ and $-1/2V_{dc}$. The line-line voltages of two legs with the capacitors are: V_{dc}, $1/2V_{dc}$, 0, $-1/2V_{dc}$ and $-V_{dc}$. Considering this arrangement to be a single leg and in order to generate a three phase voltage, three similar legs are required.

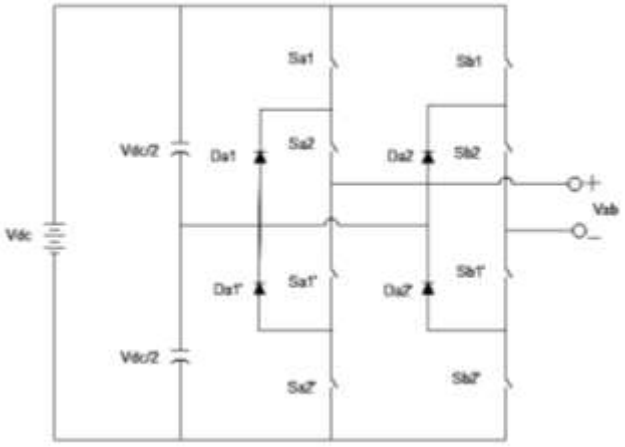

Fig 2: DC - MLI with three phase output voltage

When the number of levels increases, the number of diodes and switches used also increases. It becomes impossible to increase the number beyond a limit. As the number of levels n increases, then the number of diodes required tops on to (n-1)(n-2) diodes per phase with equal blocking voltages for all diodes.

In fig 2, the switches (Sa1 and Sa1'), (Sa2 and Sa2'), (Sb1 and Sb1') and (Sb2 and Sb2') are complimentary to each other. They should not be turned on together. Table 1 shows the switching states for the 5 – level DC MLI shown in fig 2.

Sa1	**Sa2**	**Sa1'**	**Sa2'**	**Sb1**	**Sb2**	**Sb1'**	**Sb2'**	$\mathbf{V_{ao}}$	$\mathbf{V_{bo}}$	$\mathbf{V_{ab}}$
0	0	1	1	1	1	0	0	$-V_{dc}/2$	$V_{dc}/2$	$-V_{dc}$
0	0	1	1	0	1	1	0	$-V_{dc}/2$	0	$-V_{dc}/2$
1	1	0	0	1	1	0	0	$V_{dc}/2$	$V_{dc}/2$	0
0	0	1	1	0	0	1	1	$-V_{dc}/2$	$-V_{dc}/2$	0
0	1	1	0	0	0	1	1	0	$-V_{dc}/2$	$V_{dc}/2$
1	1	0	0	0	0	1	1	$V_{dc}/2$	$-V_{dc}/2$	V_{dc}

Table 1: Switching States for 5 level DC-MLI

The advantages for the diode-clamped inverter are,

- A large number of levels 'n' yields a small harmonic distortion
- All of the phases share a common dc bus

- Reactive power flow can be controlled
- High efficiency for fundamental switching frequency
- Relatively simple control methods

The disadvantages are,

- Different voltage ratings for clamping diodes are required
- Real power flow is difficult because of the capacitors imbalance
- Need high voltage rating diodes to block the reverse voltages
- The number of switches, capacitors, and diodes required in the circuit increases with the increase in the number of output voltage levels. Extra clamping diodes required are (n-1)(n-2) per phase

III. Flying Capacitor Multilevel Inverter

The flying capacitor MLI is also known as Capacitor Clamped MLI. This topology of MLI provides more flexibility in waveform synthesis and balancing voltage. The FC – MLI topology is obtained by replacing the diodes in DC – MLI with appropriate values of capacitors. Redundancy in switching states can be availed in this topology.

Similar to the DC – MLI topology, the FC – MLI topology also has complimentary switches. In fig 3, the switches (Sa1 and Sa1'), (Sa2 and Sa2'), (Sb1 and Sb1') and (Sb2 and Sb2') are complimentary to each other. They should not be turned on together. Table 2 shows the switching states for the 5 – level FC MLI shown in fig 3

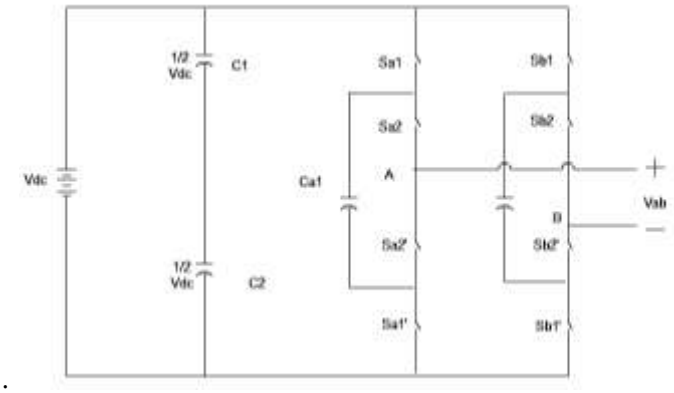

Fig 3: 5 level FC MLI

Sa1	Sa2	Sa1'	Sa2'	Sb1	Sb2	Sb1'	Sb2'	V_{ao}	V_{bo}	V_{ab}
0	0	1	1	1	1	0	0	$-V_{dc}/2$	$V_{dc}/2$	$-V_{dc}$
0	0	1	1	0	1	1	0	$-V_{dc}/2$	0	$-V_{dc}/2$
0	1	1	0	1	1	0	0	0	$V_{dc}/2$	$-V_{dc}/2$
1	0	0	1	1	1	0	0	0	$V_{dc}/2$	$-V_{dc}/2$
1	1	0	0	1	1	0	0	$V_{dc}/2$	$V_{dc}/2$	0
0	0	1	1	0	0	1	1	$-V_{dc}/2$	$-V_{dc}/2$	0
0	1	1	0	0	0	1	1	0	$-V_{dc}/2$	$V_{dc}/2$
1	1	0	0	0	1	1	0	$V_{dc}/2$	0	$V_{dc}/2$
1	0	0	1	0	0	1	1	0	$-V_{dc}/2$	$V_{dc}/2$
1	1	0	0	0	0	1	1	$V_{dc}/2$	$-V_{dc}/2$	V_{dc}

Table 2: Switching States for 5 level FC-MLI

The main advantage of FC – MLI are:

- Large 'n' allows the capacitors extra energy during long discharge transient
- Phase redundancies are available for balancing the voltage levels of the capacitors
- Lower Total Harmonic Distortion when the number of levels 'n' is high
- Active and Reactive power flow can be controlled

The disadvantages of FC – MLI are:

- Large numbers of capacitors are bulky and more expensive than the clamping diodes used in the diode-clamped multilevel inverter
- Complex control is required to maintain the capacitor's voltage balance
- Switching utilization and Efficiency are poor for real power transmission

IV. Cascaded H – Bridge Multilevel Inverter

Cascaded H – Bridge MLI is the most advanced topology of MLIs available. It uses a series string of single-phase full-bridge inverters to construct multilevel phase legs with separate dc sources.The output of each H-bridge can have three discrete levels. Higher levels can be obtained by cascaded connection of these H – Bridge units and the resultant output to be the integrated sum of these individual units. Fig 4 shows a 5 level CHB MLI with two H – Bridge units in cascaded operation. Here the switch pairs (Sa1 and Sa4), (Sa2 and Sa3), (Sb1 and Sb4) and (Sb2 and Sb3) are complimentary switches. They should not be turned on together. The switching table for fig 4 is shown in table 3. Because of its advantages, this topology of inverters have been in use to a great extent.

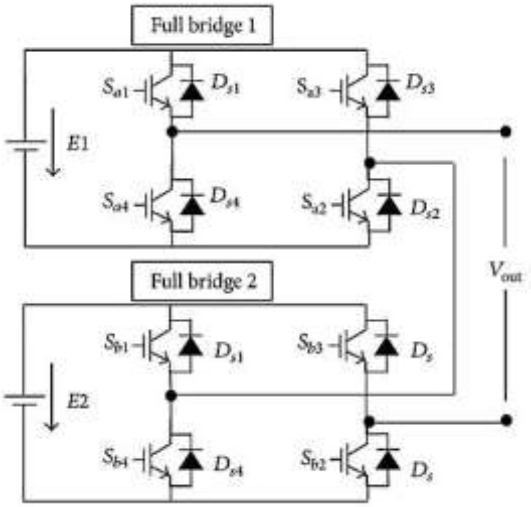

Fig 4: 5 level Cascaded H - Bridge MLI

S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{b1}	S_{b2}	S_{b3}	S_{b4}	V_{ab}
1	1	0	0	0	0	1	1	0
1	0	0	1	1	0	0	1	0
1	0	0	1	0	1	1	0	0
0	1	1	0	1	0	0	1	0
0	1	1	0	0	1	1	0	0
0	0	1	1	1	1	0	0	0
1	1	0	0	1	0	0	1	V_{dc}
1	1	0	0	0	1	1	0	V_{dc}
1	0	0	1	1	1	0	0	V_{dc}
0	1	1	0	1	1	0	0	V_{dc}
1	1	0	0	1	1	0	0	$2\ V_{dc}$
0	0	1	1	1	0	0	1	$-\ V_{dc}$
0	0	1	1	0	1	1	0	$-\ V_{dc}$
1	0	0	1	0	0	1	1	$-\ V_{dc}$
0	1	1	0	0	0	1	1	$-\ V_{dc}$
0	0	1	1	0	0	1	1	$-2\ V_{dc}$

Table 3: Switching states for 5 level CHB MLI

The advantages for cascaded multilevel H-bridge inverter are:

- The series structure allows a scalable, modularized circuit layout and packaging due to the identical structure of each H – Bridge
- No extra clamping diodes or voltage balancing capacitors are necessary
- Switching redundancy for inner voltage levels is possible because the phase voltage is the sum of the output of each bridge.

The disadvantage for cascaded multilevel H-bridge inverter is:

- Needs separate DC sources

V. Recent Trends IN MLI

The recent trends in Multilevel Inverter are focused on the reduction of size and cost of the inverter. Thereby it reduces the components used in it and hence makes it easier to handle. Another major area where the study of these types of inverters has been focused on the control mechanisms incorporated in it.

In [16], the conventional cascaded multilevel inverter with two different algorithms has been presented. These algorithms comprises of symmetric cascaded multilevel inverters and the asymmetric ones with the binary method for determining the magnitude of dc voltage sources. In [17]-[19], three different structures for the cascaded multilevel inverter have been presented.

After the literature review on these selected papers on the basis of number of steps with the number of switches, it was observed that the number of switches is less for [16] for the same number of steps when compared with the others. On comparing the number of dc voltage sources used, it has been found that the [16] has the less number of sources being used to generate the same number of steps.

VI. Conclusion

Nowadays, multilevel inverters are becoming increasingly popular in power applications, as multilevel inverters have the ability to meet the increasing demand of power rating and power quality associated with reduced harmonic distortion and lower electromagnetic interference.On this basis several topologies of MLIs have been studied. On tabulating the results as in table 4, it is found that the CHB MLI is best of all the available topologies.

Components	**CHB – MLI**	**FC – MLI**	**DC – MLI**
Switch	2(m-1)	2(m-1)	2(m-1)
Capacitors	0	[(m-1)(m-2)/2]+(m+1)]	(m-1)
Diodes	0	0	(m-1)(m-2)

Table 4: Comparison of topologies

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